



STM32F101xx and STM32F103xx Errata sheet

STM32F101xx and STM32F103xx Medium-density device limitations

Silicon identification

This errata sheet applies to the revisions B, Z and Y of the STMicroelectronics STM32F101xx access line and STM32F103xx performance line Medium-density products. These families feature an ARM™ 32-bit Cortex®-M3 core, for which an errata notice is also available (see [Section 1](#) for details).

The full list of root part numbers is shown in [Table 2](#).

The products are identifiable as shown in [Table 1](#):

- by the Revision code marked below the Sales Type on the device package
- by the last three digits of the Internal Sales Type printed on the box label

Table 1. Device Identification⁽¹⁾

| Sales type | Revision code ⁽²⁾ marked on device |
|---------------|-----------------------------------------------|
| STM32F103xxxx | "B" |
| | "Z" |
| | "Y" |
| STM32F101xxxx | "B" |
| | "Z" |
| | "Y" |

1. The REV_ID bits in the DBGMCU_IDCODE register show the revision code of the device (see the STM32F10xxx reference manual for details on how to find the revision code).

2. Refer to [Appendix A: Revision code on device marking](#) for details on how to identify the Revision code on the different packages.

Table 2. Device summary

| Reference | Part number |
|-------------|---------------------------------------------------|
| STM32F101xx | STM32F101C6, STM32F101R6, STM32F101T6 |
| | STM32F101C8, STM32F101R8 STM32F101V8, STM32F101T8 |
| | STM32F101RB, STM32F101VB, STM32F101CB |
| STM32F103xx | STM32F103C6, STM32F103R6, STM32F103T6 |
| | STM32F103C8, STM32F103R8 STM32F103V8, STM32F103T8 |
| | STM32F103RB STM32F103VB, STM32F103CB |

1 ARM™ 32-bit Cortex®-M3 limitations

An errata notice of the STM32F10xxx core is available from the following web address:

<http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.eat0420a/>.

The direct link to the errata notice pdf is:

<http://infocenter.arm.com/help/topic/com.arm.doc.eat0420a/Cortex-M3-Errata-r1p1-v0.2.pdf>.

All the described limitations are minor and related to the revision r1p1-01rel0 of the Cortex-M3 core.

2 STM32F10xxx silicon limitations

2.1 Voltage glitch on ADC input 0

Description

A low-amplitude voltage glitch may be generated (on ADC input 0) on the PA0 pin, when the ADC is converting with injection trigger. It is generated by internal coupling and synchronized to the beginning and the end of the injection sequence, whatever the channel(s) to be converted.

The glitch amplitude is less than 150 mV with a typical duration of 10 ns (measured with the I/O configured as high-impedance input and left unconnected). If PA0 is used as a digital output, this has no influence on the signal. If PA0 is used as a digital input, it will not be detected as a spurious transition, providing that PA0 is driven with an impedance lower than 5 kΩ. This glitch does not have any influence on the remaining port A pin or on the ADC conversion injection results, in single ADC configuration.

When using the ADC in dual mode with injection trigger, and in order to avoid any side effect, it is advised to distribute the analog channels so that Channel 0 is configured as an injected channel.

Workaround

None.

2.2 Flash memory read after WFI/WFE instruction

Conditions

- Flash prefetch on
- Flash memory timing set to 2 wait states
- FLITF clock stopped in Sleep mode

Description

If a WFI/WFE instruction is executed during a Flash memory access and the Sleep duration is very short (less than 2 clock cycles), the instruction fetch from the Flash memory may be corrupted on the next wakeup event.

Workaround

When using the Flash memory with two wait states and prefetch on, the FLITF clock must *not* be stopped during the Sleep mode – the FLITFEN bit in the RCC_AHBENR register must be set (keep the reset value).

2.3 Debug registers cannot be read by user software

Description

The DBGMCU_IDCODE and DBGMCU_CR debug registers are accessible only in debug mode (not accessible by the user software). When these registers are read in user mode, the returned value is 0x00.

Workaround

None.

2.4 Alternate function

In some specific cases, some potential weakness may exist between alternate functions mapped onto the same pin.

2.4.1 USART1_RTS and CAN_TX

Conditions

- USART1 is clocked
- CAN is not clocked
- I/O port pin PA12 is configured as an alternate function output.

Description

Even if CAN_TX is not used, this signal is set by default to 1 if I/O port pin PA12 is configured as an alternate function output.

In this case USART1_RTS cannot be used.

Workaround

When USART1_RTS is used, the CAN must be remapped to either another IO configuration when the CAN is used, or to the unused configuration (CAN_REMAP[1:0] set to “01”) when the CAN is not used.

2.4.2 SPI1 in slave mode and USART2 in synchronous mode

Conditions

- SPI1 and USART2 are clocked
- I/O port pin PA4 is configured as an alternate function output.

Description

USART2 cannot be used in synchronous mode (USART2_CK signal), if SPI1 is used in slave mode.

Workaround

None.

2.4.3 SPI1 in master mode and USART2 in synchronous mode

Conditions

- SPI1 and USART2 are clocked
- I/O port pin PA4 is configured as an alternate function output.

Description

USART2 cannot be used in synchronous mode (USART2_CK signal) if SPI1 is used in master mode and SP1_NSS is configured in software mode. In this case USART2_CK is not output on the pin.

Workaround

In order to output USART2_CK, the SSOE bit in the SPI1_CR2 register must be set to configure the pin in output mode.

2.4.4 SPI2 in slave mode and USART3 in synchronous mode

Conditions

- SPI2 and USART3 are clocked
- I/O port pin PB12 is configured as an alternate function output.

Description

USART3 cannot be used in synchronous mode (USART3_CK signal) if SPI2 is used in slave mode.

Workaround

None.

2.4.5 SPI2 in master mode and USART3 in synchronous mode

Conditions

- SPI2 and USART3 are clocked
- I/O port pin PB12 is configured as an alternate function output.

Description

USART3 cannot be used in synchronous mode (USART3_CK signal) if SPI2 is used in master mode and SP2_NSS is configured in software mode. In this case USART3_CK is not output on the pin.

Workaround

In order to output USART3_CK, the SSOE bit in the SPI2_CR2 register must be set to configure the pin in output mode,

2.4.6 I2C2 with SPI2 and USART3

Conditions

- I2C2 and SPI2 are clocked together or I2C2 and USART3 are clocked together
- I/O port pin PB12 is configured as an alternate function output

Description

- Conflict between the I2C2 SMBALERT signal (even if this function is not used) and SPI2_NSS in output mode.
- Conflict between the I2C2 SMBALERT signal (even if this function is not used) and USART3_CK.
- In these cases the I/O port pin PB12 is set to 1 by default if the I/O alternate function output is selected and I2C2 is clocked.

Workaround

I2C2 SMBALERT can be used as an output if SPI2 is configured in master mode with NSS in software mode.

I2C2 SMBALERT can be used in input mode if SPI2 is configured in master or slave mode with NSS managed by software.

SPI2 cannot be used in any other configuration when I2C2 is being used.

USART3 must *not* be used in synchronous mode when I2C2 is being used.

2.4.7 I2C1 with SPI1 remapped and used in master mode

Conditions

- I2C1 and SPI1 are clocked.
- SPI1 is remapped.
- I/O port pin PB5 is configured as an alternate function output.

Description

Conflict between the SPI1 MOSI signal and the I2C1 SMBALERT signal (even if SMBALERT is not used).

Workaround

Do not use SPI1 remapped in master mode and I2C1 together.

When using SPI1 remapped, the I2C1 clock must be disabled.

2.4.8 I2C1 and TIM3_CH2 remapped**Conditions**

- I2C1 and TIM3 are clocked.
- I/O port pin PB5 is configured as an alternate function output.

Description

Conflict between the TIM3_CH2 signal and the I2C1 SMBALERT signal, (even if SMBALERT is not used).

In these cases the I/O port pin PB5 is set to 1 by default if the I/O alternate function output is selected and I2C1 is clocked. TIM3_CH2 cannot be used in output mode.

Workaround

To avoid this conflict, TIM3_CH2 can only be used in input mode.

Appendix A Revision code on device marking

[Figure 1](#), [Figure 2](#), [Figure 3](#) and [Figure 4](#) show the marking compositions for the LQFP100, LQFP64, LQFP48 and VFQFPN36 packages, respectively. Only the Additional field containing the Revision code is shown.

Figure 1. LQFP100 top package view

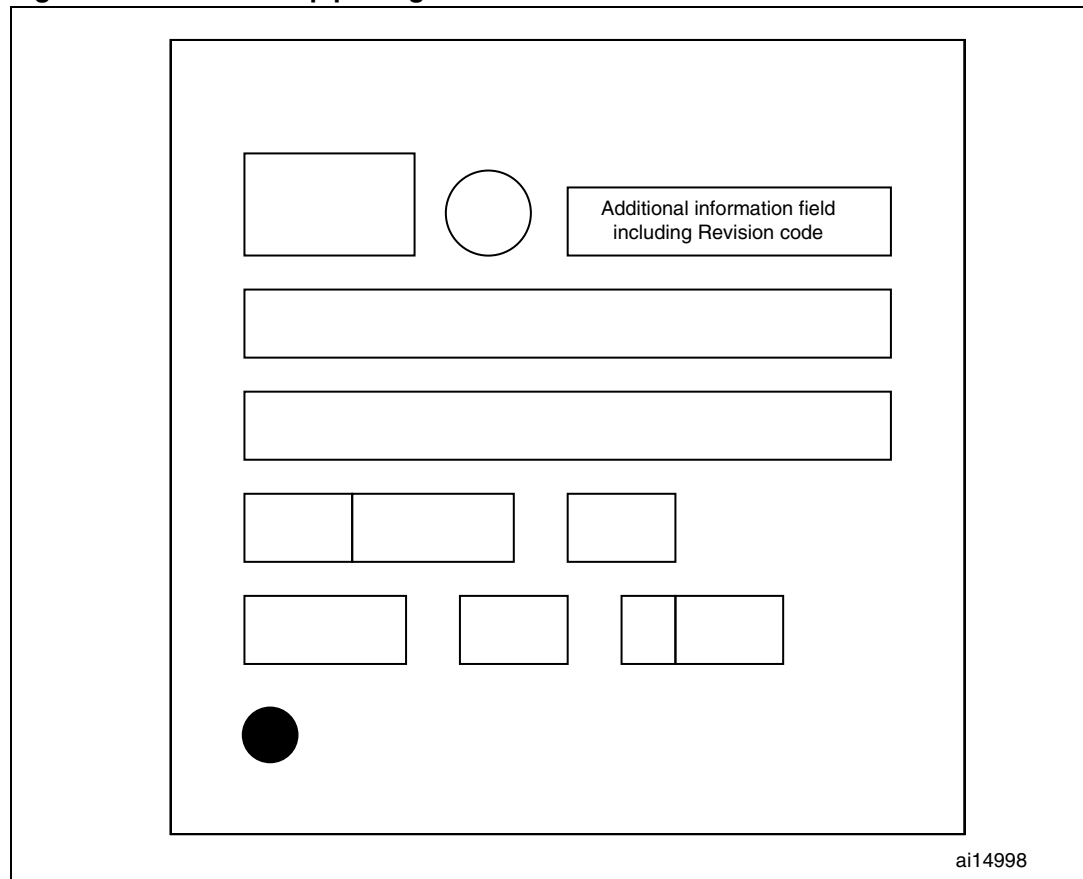


Figure 2. LQFP64 top package view

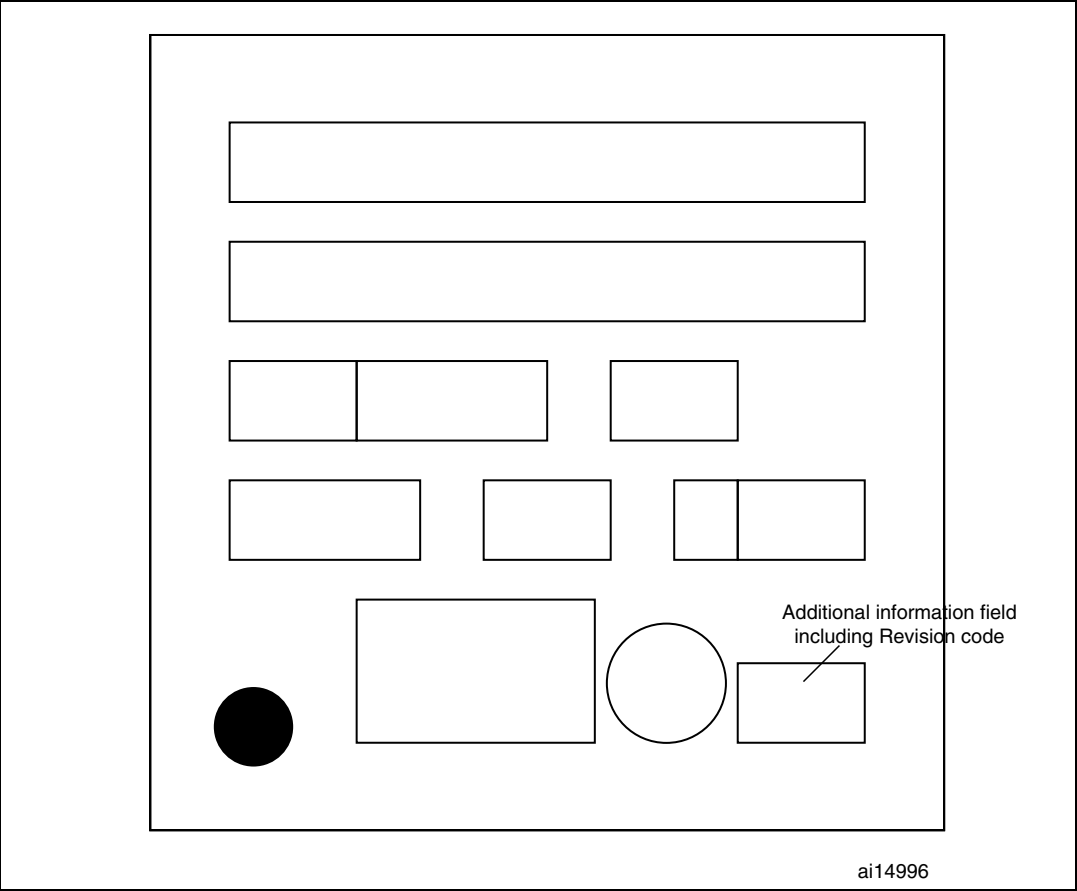


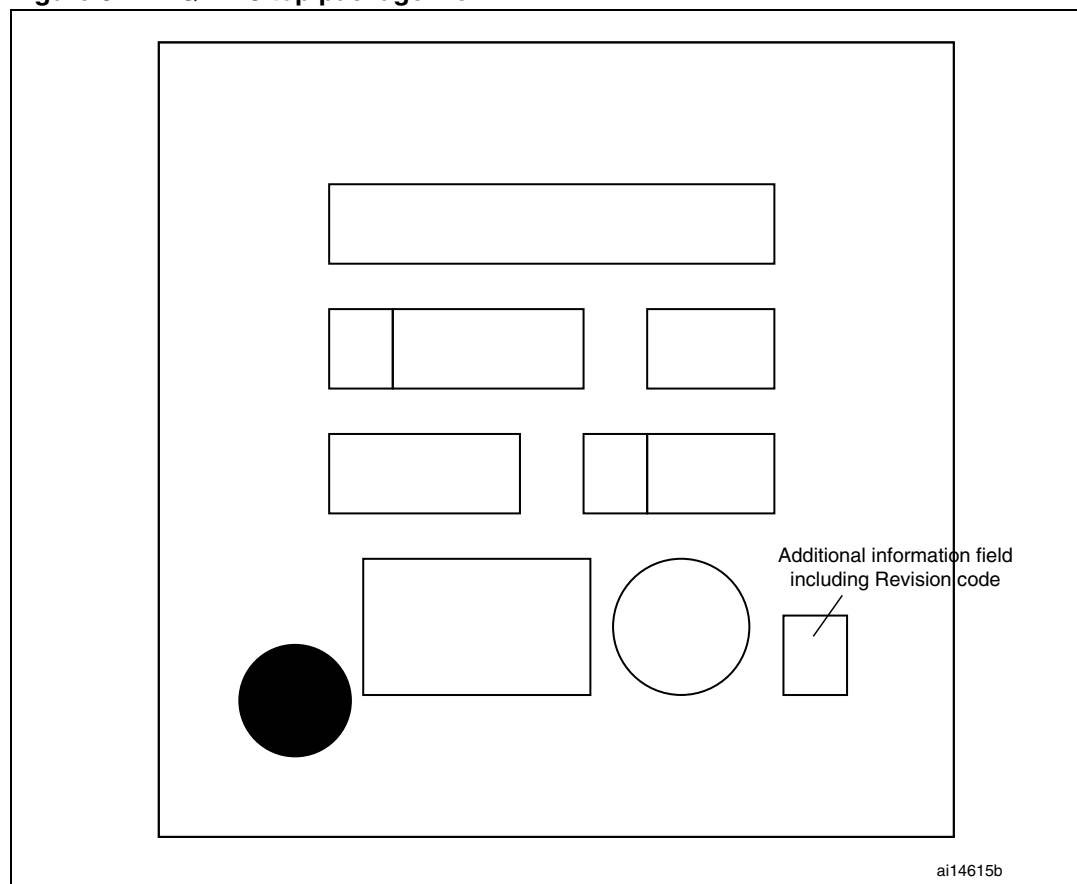
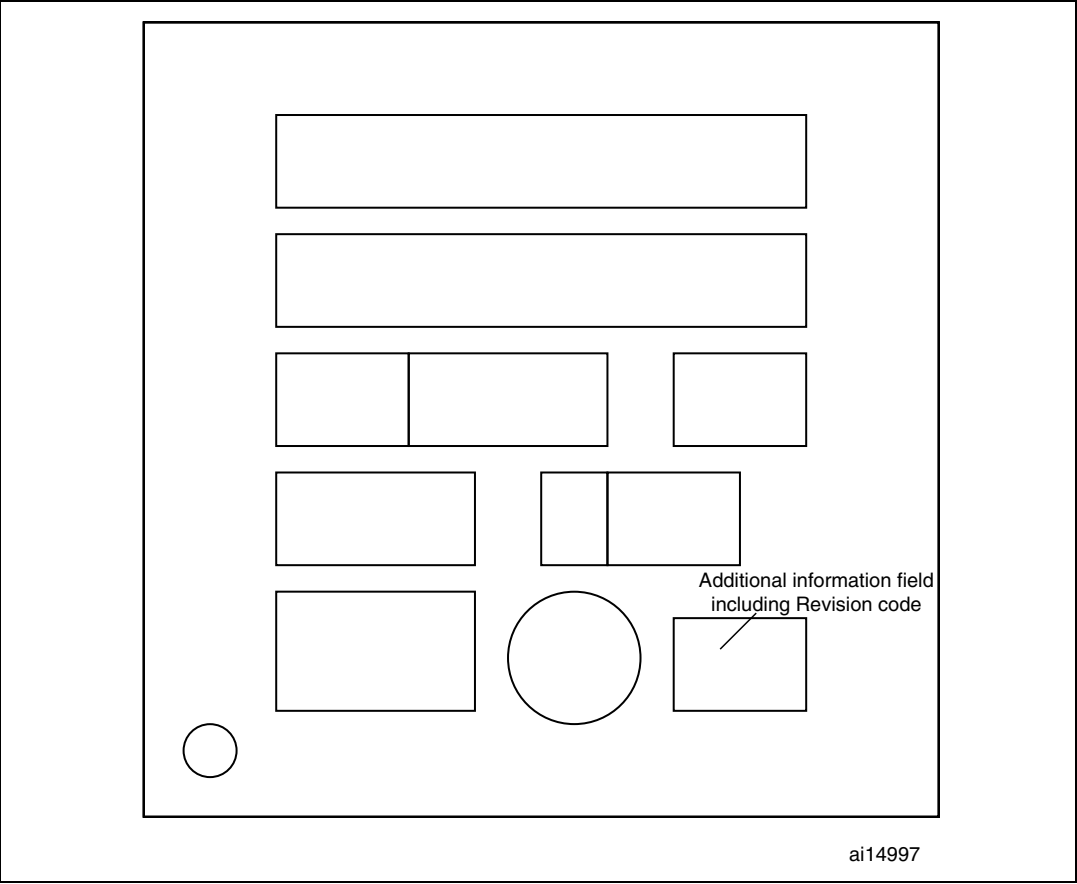
Figure 3. LQFP48 top package view

Figure 4. VFQFPN36 top package view



Revision history

Table 3. Document revision history

| Date | Revision | Changes |
|-------------|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 28-Mar-2008 | 1 | Initial release. |
| 07-Apr-2008 | 2 | <i>Section 2.2: Flash memory read after WFI/WFE instruction on page 2</i> added. Workaround specified in <i>Section 2.4.1: USART1_RTS and CAN_TX</i> . |
| 23-May-2008 | 3 | The errata sheet also applies to Revision Y devices. <i>Section 2.1: PD0 and PD1 use in output mode</i> , <i>Section 2.2: ADC auto-injection channel</i> and <i>Section 2.3: ADC combined injected simultaneous+interleaved</i> removed from errata sheet. <i>Section 2.3: Debug registers cannot be read by user software on page 3</i> added. Small text changes. |

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS EXPRESSLY APPROVED IN WRITING BY AN AUTHORIZED ST REPRESENTATIVE, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER'S OWN RISK.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2008 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com